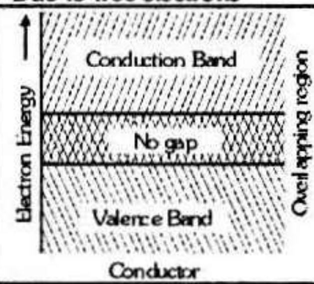
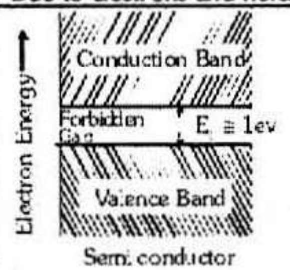
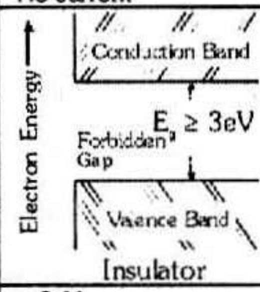
Comparison between conductor, semiconductor and insulator :

Properties	Conductor	Semiconductor	Insulator
Resistivity	$10^{-2} - 10^{-8}\ \Omega m$	$10^{-5} - 10^{6}\ \Omega m$	$10^{11} - 10^{19}\ \Omega m$
Conductivity	$10^{2} - 10^{8}$ mho/m	$10^{5} - 10^{-6}$ mho/m	$10^{-11} - 10^{-19}$ mho/m
Temp. Coefficient of resistance (α)	Positive	Negative	Negative
Current	Due to free electrons	Due to electrons and holes	No current
Energy band diagram			
Forbidden energy gap	$\cong 0eV$	$\cong 1eV$	$\geq 3eV$
Example	Pt, Al, Cu, Ag	Ge, Si, GaAs, GaF_2	Wood, plastic, Diamond, Mica

- **Number of electrons reaching from valence band to conduction band**

$$n = AT^{3/2} e^{-\frac{\Delta E_g}{2kT}}$$

- **Classification of Semiconductors :**

SEMICONDUCTOR

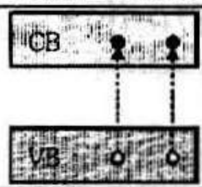
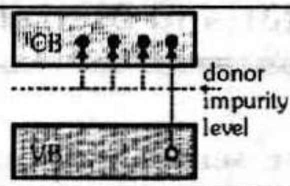
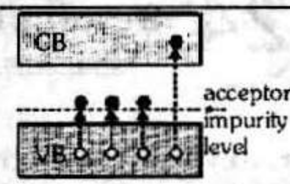
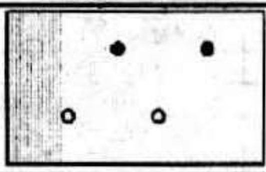
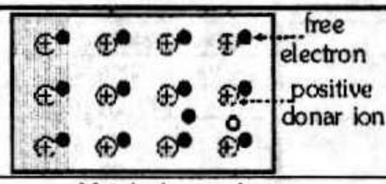
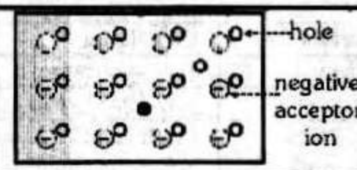
- Intrinsic semiconductor
  - (pure form of Ge, Si)
  - $n_e = n_h = n_i$
- Extrinsic semiconductor (doped semicondutor)
  - N-type
    - pentavalent impurity
    - (P, As, Sb etc.)
    - donar impurity (N_D)
    - $n_e >> n_h$
  - P-type
    - trivalent impurity
    - (Ga, B, In, Al)
    - acceptor impurity (N_A)
    - $n_h >> n_e$

- **Mass-action law** $n_i^2 = n_e \times n_h$

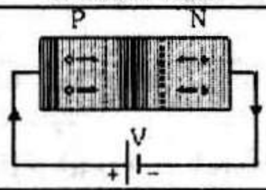
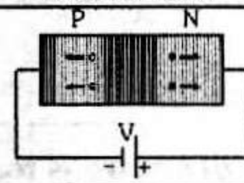
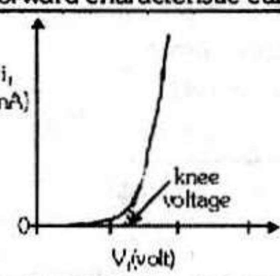
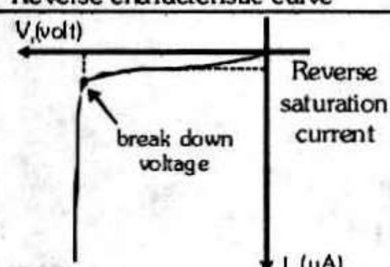
  ❑ For N-type semiconductor $n_e = N_D$

  ❑ For P-type semiconductor $n_h = N_A$

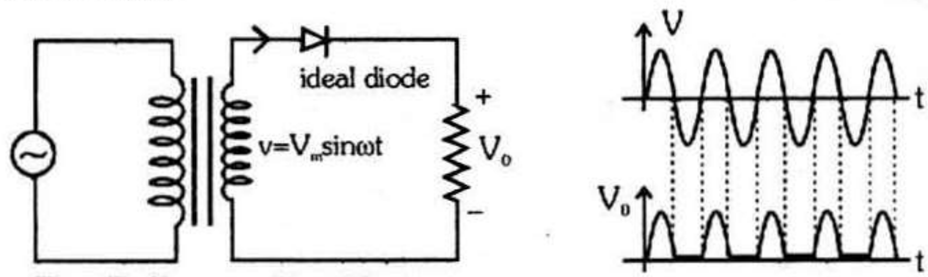
- **Conductivity** $n_i e(\mu_e + \mu_h)$

Intrinsic Semiconductor	**N-type (Pentavalent impurity)**	**P-type (Trivalent impurity)**
		
		
Current due to electron and hole	Mainly due to electrons	Mainly due to holes
$n_e = n_h = n_i$	$n_h << n_e$ $(N_D \simeq n_e)$	$n_h >> n_e$ $(N_A \simeq n_h)$
$I = I_e + I_h$	$I \simeq I_e$	$I \simeq I_h$
Entirely neutral	Entirely neutral	Entirely neutral
Quantity of electrons and holes are equal	Majority – Electrons Minority – Holes	Majority – Holes Minority - Electrons

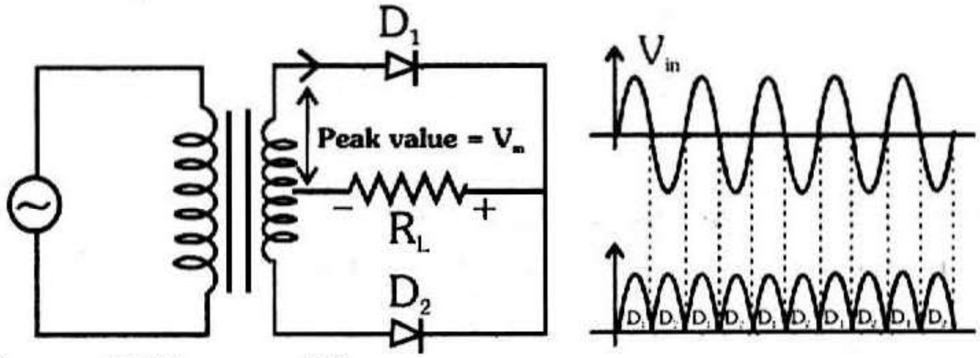
Comparison between Forward Bias and Reverse Bias

	Forward Bias		**Reverse Bias**
			
1	Potential Barrier reduces	1	Potential Barrier increases.
2	Width of depletion layer decreases	2	Width of depletion layer increases.
3	P-N jn. provide very small resistance	3	P-N jn. provide high resistance
4	Forward current flows in the circuit	4	Very small current flows.
5	Order of forward current is milli ampere.	5	Order of current is micro ampere for Ge or Neno ampere for Si.
6	Current flows mainly due to majority carriers.	6	Current flows mainly due to minority carriers.
7	Forward characteristic curves.	7	Reverse characteristic curve
			
8	Forward resistance : $R_f = \frac{\Delta V_f}{\Delta I_f} \cong 100\Omega$	8	Reverse resistance : $R_r = \frac{\Delta V_r}{\Delta I_r} \cong 10^6\Omega$
9	Order of knee or cut in voltage	9	Breakdown voltage
	Ge→ 0.3 V		Ge → 25 V
	Si → 0.7 V		Si → 35 V
	Special point : Generally $\frac{R_r}{R_f} = 10^3 : 1$ for Ge		$\frac{R_r}{R_f} = 10^4 : 1$ for Si

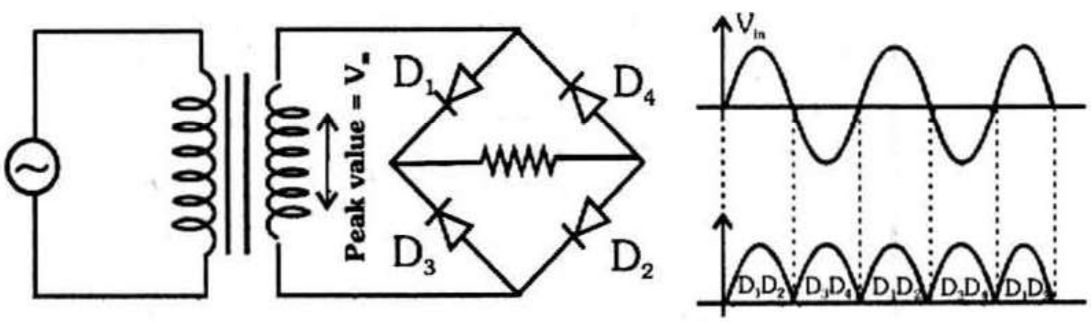
- **Half wave rectifier**



- **Centre – Tap Full wave Rectifier**



- **Full wave Bridge reactifier**

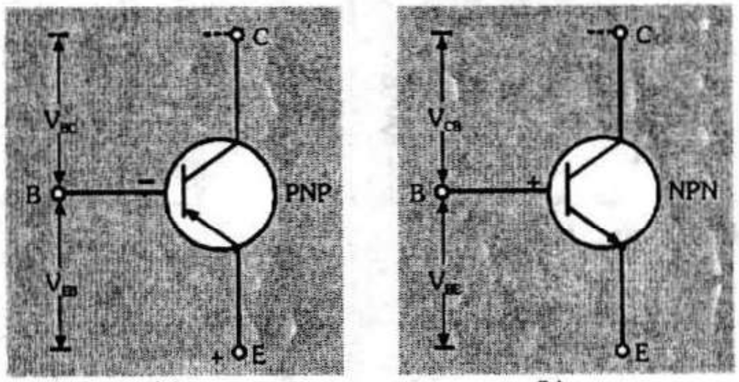


- **Form factor** $= \dfrac{I_{rms}}{I_{dc}}$
  - ❐ For HWR (Half wave rectifier) Form factor $= \dfrac{\pi}{2}$
  - ❐ For FWR (Full wave rectifier) Form factor $= \dfrac{\pi}{2\sqrt{2}}$

- **Ripple factor** $r = \dfrac{I_{ac}}{I_{dc}}$
  - ❐ For HWR $r = 1.21$ ❐ For FWR $r = 0.48$

- **Rectifier efficiency** $\eta = \dfrac{P_{dc}}{P_{ac}} = \dfrac{I_{dc}^2 R_L}{I_{rms}^2 (R_F + R_L)}$
  - ❐ For HWR $\eta\% = \dfrac{40.6}{1 + \dfrac{R_F}{R_L}}$ & FWR $\eta\% = \dfrac{81.2}{1 + \dfrac{R_F}{R_L}}$

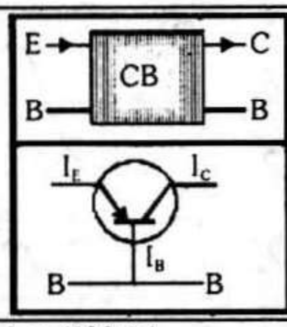
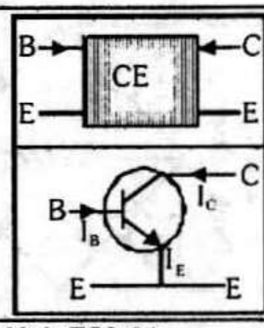
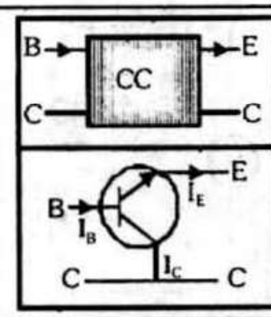
- **For transistor** $I_E = I_B + I_C$



(a) (b)

Comparative study of transistor configurations

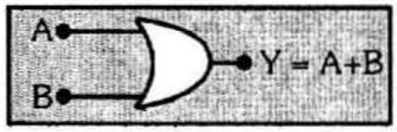
1. Common Base **(CB)**
2. Common Emitter **(CE)**
3. Common Collector **(CC)**

	CB	**CE**	**CC**
			
Input Resistance	Low (100 Ω)	High (750 Ω)	Very High ≅ 750 kΩ
Output resistance	Very High	High	Low
Current Gain	(A_I or α)	(A_I or β)	(A_I or γ)
	$\alpha = \frac{I_C}{I_E} < 1$	$\beta = \frac{I_C}{I_B} > 1$	$\gamma = \frac{I_E}{I_B} > 1$
Voltage Gain	$A_V = \frac{V_o}{V_i} = \frac{I_C R_L}{I_E R_i}$	$A_V = \frac{V_o}{V_i} = \frac{I_C R_L}{I_B R_i}$	$A_V = \frac{V_o}{V_i} = \frac{I_E R_L}{I_B R_i}$
	$A_v = \alpha \frac{R_L}{R_i} \cong 150$	$A_v = \beta \frac{R_L}{R_i} \cong 500$	$A_v = \gamma \frac{R_L}{R_i} < 1$
Power Gain	$A_p = \frac{P_o}{P_i} = \alpha^2 \frac{R_L}{R_i}$	$A_p = \frac{P_o}{P_i} = \beta^2 \frac{R_L}{R_i}$	$A_p = \frac{P_o}{P_i} = \gamma^2 \frac{R_L}{R_i}$
Phase difference (between output and input)	same phase	opposite phase	same phase
Application	For High Frequency	For Audible frequency	For Impedance Matching

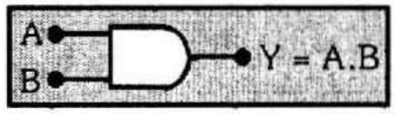
- **Relation between α, β and γ :** $\beta = \frac{\alpha}{1-\alpha}$, $\gamma = 1 + \beta$, $\gamma = \frac{1}{1-\alpha}$

- **Logic gates**

  - OR gate

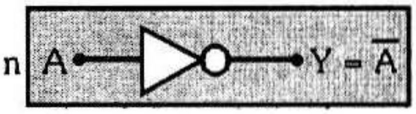


  - AND gate

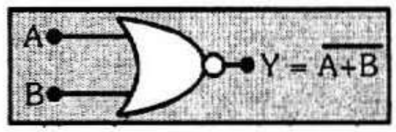


  - NOT gate

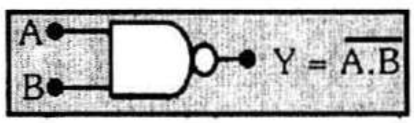
n



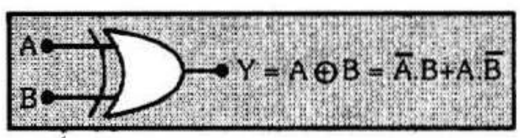
  - NOR gate



  - NAND gate



  - XOR gate



  - XNOR gate

- **De Morgan's theorem** $\overline{A+B} = \bar{A} \cdot \bar{B}$, $\overline{A \cdot B} = \bar{A} + \bar{B}$

OR	AND	NOT
$A + 0 = A$	$A. 0 = 0$	$A + \bar{A} = 1$
$A + 1 = 1$	$A. 1 = A$	$A \cdot \bar{A} = 0$
$A + A = A$	$A . A = A$	$\bar{\bar{A}} \cdot A = A$

Important notes